

[0027] Figure 2 is a schematic cross-sectional view of the CMOS image pixel cell of FIG. 1 taken along line 2-2'.

[0028] Figure 3A is a top plan view of an exemplary CMOS image pixel cell with a photodiode spaced from the photodiode's active area.

[0029] Figure 3B is a schematic cross-sectional view of the CMOS image pixel cell of FIG. 3A taken along line 2-2'.

[0030] Figure 4A is a top plan view of an exemplary CMOS image pixel cell with a photodiode overlapping the photodiode's active area.

[0031] Figure 4B is a schematic cross-sectional view of the CMOS image pixel cell of FIG. 4A taken along line 2-2'.

[0032] Figure 5A is a schematic cross-sectional view of a CMOS image pixel cell illustrating a photodiode and isolation region formed in accordance with one exemplary embodiment of the present invention.

[0033] Figure 5B is a schematic cross-sectional view of the CMOS image pixel cell of FIG. 5A taken along line 2-2' illustrating a photodiode and isolation region formed in accordance with one exemplary embodiment of the present invention.

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[0034] Figures 6A-^{6M}~~6E~~ are schematic cross-sectional views of the CMOS image pixel cell fragment of FIGS. 5A illustrating one exemplary fabrication embodiment of the photodiode and isolation region in accordance with the present invention.

[0035] Figure 7 is a schematic cross-sectional views of the CMOS image pixel cell of FIG. 5A at a stage of processing subsequent to that shown in FIGS. 6A-6E.